REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1, 2, 4-8, 10-13 and 15-19 remain active in this case, Claims 1, 7, 13, and 16 having been amended and Claims 3, 9 and 14 canceled by the present amendment.

Claims 1-4, 7-10 and 13-15 stand finally rejected under 35 U SC 102(b) as being anticipated by Stolmeijer et al (U.S. 5,742,090); and Claims 5, 6, 11, 12 and 17-19 were rejected under 35 USC §103(a) as being unpatentable over Stolmeijer et al.

Applicant acknowledges with appreciation the courtesy of the interview granted to Applicants' attorney on April 29, 2003, at which time the outstanding grounds for rejection were discussed. In particular, during the interview the Examiner explained his reasoning, relying on column 3, lines 9-12, lines 23-29, and lines 59-65 of Stolmeijer et al that the presently pending independent claims are anticipated by Stolmeijer et al. The Examiner explained that in Figure 5 Stolmeijer et al disclose a well region 230 formed by an active region 210 and a field region 220, and that Stolmeijer et al at column 3, lines 11-12 state that "an active region 210 and a field region 220 is defined with respect to the active device 200," and at column 3, lines 26-28 that "the field region 220 of the n-well region 230 is implanted with n+ impurities... ." The Examiner further explained that because the field region 220 is implanted with impurities, at a depth in the device within the field region, in the absence of any indication that the active region 210 is also implanted, the Examiner considered that a portion of the field region 220 has a lower resistance value than that of the active region 210 in the well region 230 of the Stolmeijer et al Figure 5 device. No agreement was reached during the interview.

In light of the discussions during the interview, and to expedite examination, Claim 1 has been amended to include the features formerly stated in Claim 3; Claim 6 has been amended to include the features formerly stated in Claims 9; and Claim 13 has been amended to include the features formerly stated in Claim 14. Claims 3, 9 and 14 have therefore been canceled. Claim 16 has also been amended to clarify structure believed to be more clearly patentably distinguishing over Stolmeijer et al. No new matter has been added.

Turning now to the teachings of Stolmeijer et al, in Stolmeijer et al., the field region 220 is formed by implanting n+ impurities in the well region 230. Column 3, line 28 of Stolmeijer et al. refers to, "n+". However, the use of "n+" is not consistent. In the drawings of Stolmeijer et al., the regions which have high impurity concentration, such as source/drain regions 30 and 40 as a diffusion layer, are marked "+", but the other regions are not marked "+". Therefore, it is Applicants' view that Stolmeijer et al. do not describe a particular method for producing a well, but discloses only a general forming method thereof. That is, Stolmeijer et al. only disclose implanting "P+" or "N+" impurities in a corresponding well region and define the range of active devices. Stolmeijer et al., accordingly do not teach a structure wherein the impurity concentration at the bottom of the well is set higher than the central portion in the depth direction of the well. Applicants therefore respectfully submit that Stolmeijer et al. do not disclose the structural limitations of each of the amended claims.

Applicants further point out that, where p+ or n+ impurities are implanted in the well regions 130 and 230, the impurity concentration of the well regions 120 and 230, overall, will be approximately the same as that of the field regions 120 and 220. This means that it is difficult to produce a portion having a higher impurity concentration at the bottom of a well region, as claimed, by a mere implantation of impurities in a well region as in Stolmeijer et al., and it is necessary to determine the portion where the impurities are implanted. Stolmeijer et al., however, do not teach forming a portion having a higher impurity

concentration at the bottom of the well region. Merely implanting impurities in a field region, as taught by Stolmeijer et al does not suggest that the impurity concentration specifically at the bottom of the well region is higher.

Therefore, in the consideration of Applicants' invention, attention is directed not only to the provision of an area having higher impurity concentration in the well area, but also the position (depth) where such an area is formed. To that end, amended claims 1, 7, 13 and 16 have been amended to accentuate that the low resistance area is not in contact with a depletion layer, but in contact with the element isolation area or isolation area. Such a structure separates each of the circuit elements, without fail, as well as keeps the well resistance at a low level, thereby suppressing thermal noise. Upon application of the Applicants' invention to a variable capacitance capacitor provided in a voltage controlled oscillator, the Q value is improved, which reduces phase noise.

It is respectfully submitted that Stolmeijer et al. do not teach the position where field regions 120 and 220 are formed. Instead, at column 3, lines 9 to 12 Stolmeijer et al. merely state that the field regions 120 and 220 only define the active devices 100 and 200, as well as active regions 110 and 210. Therefore, it is respectfully submitted Stolmeijer et al. do not teach or render obvious the clarified subject matter defined by amended Claims 1, 7, 13 and 16. It is thus respectfully submitted that the amended Claims 1, 7, 13 and 16 and the claims dependent therefrom are not anticipated by or rendered obvious over Stolmeijer et al.

Consequently, in view of the present amendment and in light of the above discussion, the pending claims are believed to be in condition for allowance, and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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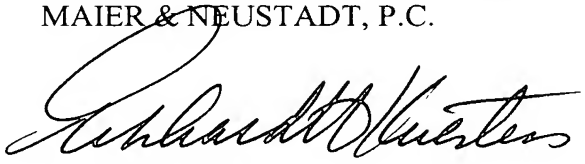

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IN THE CLAIMS

--1. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a first conductivity type well area formed in a surface area of the semiconductor substrate;

a plurality of element isolation areas formed in the well area;

a second conductivity type semiconductor layer formed at a first area of the well area which is isolated by the element isolation areas, the semiconductor layer configuring a first electrode of a capacitor; and

a first conductivity type low resistance area provided at a base portion of the well area, the low resistance area having a resistive value lower than that of the well area,

wherein the low resistance area is not in contact with a depletion layer of a junction portion between the semiconductor layer and the well area and is in contact with the element isolation areas.

7. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a first conductivity type well area formed in a surface area of the semiconductor substrate;

a plurality of element isolation areas formed in the well area;

an MOS transistor formed in a first area of the well which is isolated by the element isolation areas; and

a first conductivity type low resistance area provided at a base portion of the well area an having a resistive value lower than that of the well area,

wherein the low resistance area is not in contact with a depletion layer of a junction portion between source/drain regions of the MOS transistor and is in contact with the element isolation areas.

13. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a first conductivity type well area formed in a surface area of the semiconductor substrate;

a plurality of element isolation areas formed in the well area;

a second conductivity type base layer formed on the well area which is isolated by the element isolation areas, the well area configuring a first electrode of a bipolar transistor;

a first conductivity type second electrode formed on the base layer; and

a first conductivity type low resistance area provided at the base portion of the well area, the low resistance area having a resistive value lower than that of the well area,

wherein the low resistance area is not in contact with a depletion layer of a junction portion of the bipolar transistor and is in contact with the element isolation areas.

16. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a first well area formed in a surface area of the semiconductor substrate;

a second well area formed in a surface area of the semiconductor substrate;

an analog circuit formed in the first well area;

a digital circuit formed in the second well area; [and]

an isolation area formed between the first and second well area; and

a first conductivity type low resistance area provided at a base portion of the first well area, the first conductivity type low resistance area having a resistive value lower than that of the first well area,

wherein the low resistance area is not in contact with a depletion layer of the analog circuit and in contact with the isolation area.